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Efficient Digital Decimation Filter Designs for Improved Frequency Response in High Frequency Applications

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ABSTRACT
This paper is concerned with cascade design of CIC filter to improve the pass band droop for decimation filter. Decimation filter has wide applications in both analog and digital systems for data rate conversion as well as filtering. CIC filters satisfy linear phase filter requirements, which are required for time sensitive features like video and speech. All the filter coefficients are unity in case of CIC filters, resulting in reduced hardware requirement. In order to improve the frequency response of CIC filters, cascading of two or more CIC filters can be done with a CIC compensator filter. Hence in this paper, performance of different cascade designs of CIC filter is compared in terms of amount of passband ripple present in magnitude response and hardware requirement for WiMAX applications . The results show that passband ripple present in the magnitude response of CIC filter can be reduced using cascade design but in that case implementation cost of filter increases by a great extent.
Key Words- CIC, Compensation Technique, Decimation, Multirate filtering, WiMax

I. INTRODUCTION

Fast sampling rates offer several benefits, including their ability to digitize wideband signals, reduced complexity of anti-alias filters, and lower noise power spectral density. The result is improved SNR in the system. Digital filtering is a computational process used for transforming a discrete sequence of numbers (the input) into another discrete sequence of numbers (the output) having a modified frequency domain spectrum. Digital filtering algorithms are most commonly implemented using general purpose digital signal processing chips for higher sampling rates. The decimation filter (decimator) is one of the basic building block of a sampling rate conversion system as shown in Figure 1. The decimation filter performs two operations: low-pass filtering as well as down-sampling. It has been widely used in applications such as speech processing, radar systems, antenna systems and communication systems. Considerable attention has been focused in the last few years on the design of high efficiency decimation filters.

In [1], author invented a new class of economical digital filters for decimation and interpolation (converting the sampling rate from low to high) called a cascaded integrator comb (CIC) filter. This filter was composed of an integrator part and a comb part. No multipliers were required and the storage requirement was reduced when compared with other implementations of decimation filters. The CIC filter can also be implemented very efficiently in hardware due to its symmetric structure.

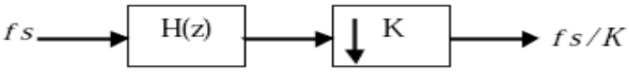

Figure 1: Conceptual View of a Decimation Filter

This filter is a combination of digital integrator and digital differentiator stages, which can perform the operation of digital low pass filtering and decimation at the same time.

A programmable decimation and interpolation digital filter based on the CIC structure is designed [2]. The circuit was configurable as either a decimation filter or an interpolation filter and the conversion ratio was programmable to any integer value from 10 to 256. The filter was designed with MOSIS 1.2 micron CMOSN standard cell libraries and data input rate could be as high as 50MHz.

In [3] a simple interpolated second-order polynomial filter (ISOP) cascaded with a CIC decimation filter to effectively reduce the pass band distortion caused by CIC filtering with little degradation in aliasing attenuation is used.

In [4], authors decomposed the decimation ratio R into two factors, namely, R1*R2 (R1 and R2 are integers)

to implement a CIC decimation filter. Instead of using one CIC filter to decimate the high speed digital signal, two CIC decimation filters: one CIC filter with a decimation ratio of R1, and one with a decimation ratio of R2 are used. The implementation of the first decimator is based on a poly phase decomposition.

Another way of implementation the CIC decimation filter is presented [5], in which the decimation factor N was constrained to an M-th power-of-two. The transfer function can be rewritten as the product of M identical low-order FIR filters. The sampling rate in this implementation decreased at every stage by a factor of two. In [6], author proposed a simple multiplier free Sin based compensator with only two adders. The proposed method is computational efficient and less complex.

A multiplierless CIC compensation filter based on the 2*M* order filter and the sharpening technique is designed [7] [8]. This technique attempts to improve the pass band and the stop band of a symmetric non recursive filter using multiple copies of the same filter. An efficient modification in the CIC cosine decimation filter is carried out [9]. The second order compensator filter is introduced at low rate in order to improve the pass band filter.

A performance evaluation of multirate filters for digital down converters is carried out [10]. The proposed filter structures have wide applications in the designing of sample rate converters, analog to digital converter, decimators and interpolators. A kind of comb filter with low power consumption is proposed [11]. This comb filter can be applied to the first stage of digital decimation filter for delta-sigma AID converter, and realize the 32 multiples frequency reducing.

A cascade design of sharpened CIC filter and polyphase structure of FIR for efficient compensation in decimation is proposed [12], which has better passband and stopband performance.

In this paper, we analyze the performance of CIC decimation filter with decimation factor 8 by cascading it to a compensation filter in two different ways to achieve a CIC decimation filter structure with an improved frequency response.

II. CASCADED INTEGRATOR COMB (CIC) FILTER

Cascaded integrator-comb (CIC), or Hogenauer filters, are multirate filters used for realizing large sample rate changes in digital systems. CIC filters are multiplierless structures, consisting of only adders and delay elements which is a great advantage when aiming at low power consumption. They are typically employed in applications that have a large excess sample rate i.e. the system sample rate is much larger than the bandwidth occupied by the signal. CIC filters are frequently used in digital down-converters (DDCs) and digital up-converters. The CIC filter is a class of hardware-efficient linear phase finite impulse response (FIR) digital filters, it consists of an equal number of stages of ideal integrator filters and comb filters. Its frequency response may be tuned by selecting the appropriate number of cascaded integrator and comb filter pairs. The highly symmetric structure of a CIC filter allows efficient implementation in hardware. However, the disadvantage of a CIC filter is that its pass band is not flat, which is undesirable in many applications. Fortunately, this problem can be alleviated by a compensation filter. CIC filters achieve sampling rate decrease (decimation) and sampling rate increase (interpolation) without using multipliers. The CIC filter first performs the averaging operation then follows it with the decimation. The transfer function of the CIC filter in z-domain is given in equation (1).

$$H[z] = H[z]_I^p . H[z]_C^p = \frac{\left(1 - z^{-K}\right)^p}{\left(1 - z^{-1}\right)^p} = \left(\frac{1 - z^{-K}}{1 - z^{-1}}\right)^p \qquad (1)$$

In equation (1), *K* is the oversampling ratio and *p* is the order of the filter. The numerator (1–*z*–*K*) ^ *p* represents the transfer function of a differentiator and the denominator 1/(1– *z* –1)^ *p* indicates the transfer function of an integrator. A simple block diagram of a first order CIC filter is shown in Figure 2. In a CIC filter, the integrators operate at high sampling frequency (*fs*), and the comb filters operate at low frequency *(fs/K)* The clock divider circuit divides the oversampling clock signal by the oversampling ratio, K after the integrator stage.

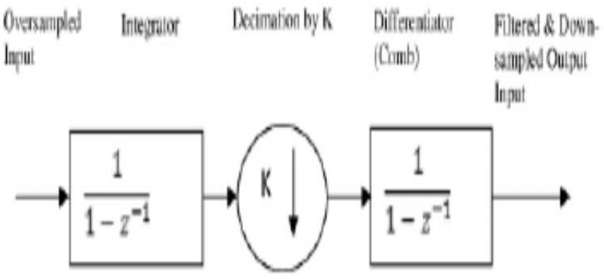

Figure 2: Block Diagram of First Order CIC Filter

By operating the differentiator at lower frequencies, a reduction in the power consumption is achieved. To ensure high system clock frequencies, the CIC decimator is actually implemented using the pipelined architecture. The pipeline registers shorten the critical path through the differentiator cascade of the basic architecture.

III. DECIMATION TECHNIQUES

3.1 Using FIR Filters

The FIR Decimation block resamples the discrete-time input at a rate K times slower than the input sample rate. The block down samples the filtered data to a lower rate by discarding (K-1) consecutive samples following every sample retained. The design of FIR filter is based on the often added requirement that the phase response be linear. FIR filter is not based on any feedback path and can easily be designed to be linear phase by making the coefficient sequence symmetric i.e. equal delay at all frequencies. This property is sometimes desired for phase-sensitive applications. The structure of a FIR filter is given in Figure 3.

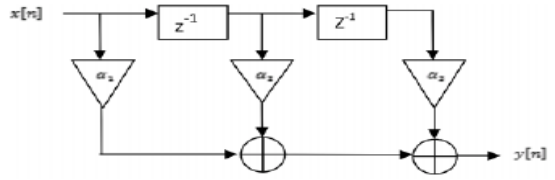

Figure 3: Structure of FIR Filter

The main disadvantage of FIR filters is that, considerably more computation power in a general purpose processor is required as compared to an Infinite impulse response (IIR) filters with similar sharpness or selectivity, especially when low frequency (relative to the sample rate) cutoffs are needed. However, many digital signal processors provide specialized hardware features to make FIR filters approximately as efficient as IIR for many applications.

3.2 Using IIR Filters

In multirate applications, the computational requirements for FIR filters can be reduced by the sampling rate conversion factor. However, such a degree of computation savings cannot be achieved in multirate implementations of IIR filters. This is due to the fact that every sample value computed in the recursive loop is needed for evaluating an output sample. Based on the polyphase decomposition, several techniques have been developed which improve the efficiency of IIR decimators and interpolators. IIR filters are used in applications where the computational efficiency is the highest priority. It is well known that an IIR filter transfer function is of a considerably lower order than the transfer function of an FIR equivalent. The drawbacks of an IIR filter are the nonlinear phase characteristic and sensitivity to quantization errors.

3.3 Using CIC Filters

These filters require no multipliers and use limited storage thereby leading to more economical hardware implementations. They are designated Cascaded Integrator-Comb (CIC) filters because their structure consists of an integrator section operating at the high sampling rate and a comb section operating at the low sampling rate. Using CIC filters, the amount of passband aliasing or imaging error can be brought within prescribed bounds by increasing the number of stages in the filter. However, the width of the passband and the frequency characteristics outside the passband are severely limited.

IV. COMPENSATION TECHNIQUE

When the number of stages is large, the CIC filter frequency response does not have a wide, flat pass band. To overcome the magnitude drop, a FIR filter with magnitude response that is the inverse of the CIC filter can be applied to achieve frequency response correction. Such filters are called "compensation filters."

In this paper, cascading of CIC filter with CIC Compensator in two different manners is carried out. The motivation behind the compensation methods is to appropriately modify the original CIC characteristic in the pass band such that the compensator filter has as low passband ripples as possible.

V. ANALYSIS AND MAGNITUDE RESPONSE

In the presented paper, magnitude responses of CIC filters are plotted using three different schemes. In the first scheme, decimation by a factor of 8 is achieved by using a single CIC Filter. Figure 4 shows the frequency response of a single stage CIC filter for decimation factor of 8. Second method makes use of cascade design of CIC Filters. A CIC filter is cascaded with a CIC Compensator. Decimation factors for the two filters are 4 and 2 respectively. Figure 5 shows the individual response of CIC filter and Compensator respectively. Figure 6 shows the overall magnitude response of the cascade design for the compensated two stage CIC filter. Another method carries out the decimation process in three stages. The decimator design consists of cascading of two CIC Filters with a CIC Compensator. The value of decimation factor is 2 and is same for all the three stages. Overall response of compensated three stage CIC filter is shown in Figure. 7. Amount of pass band ripples present in the magnitude response and cost of implementation of the filter for each method is compared. All the specifications used for the decimation process are of that of WiMAX system. Decimation filter specifications for WiMAX system are also shown in Table 1 and performance comparison is depicted in Table 2.

TABLE 1: Decimation Filter Design Parameters for WiMAX System

Input Sampling Frequency	91.392 MHz
Output Sampling Frequency	11.424 MHz
Passband Edge	4.75 MHz
Decimation Factor	8
Stopband Attenuation	90dB

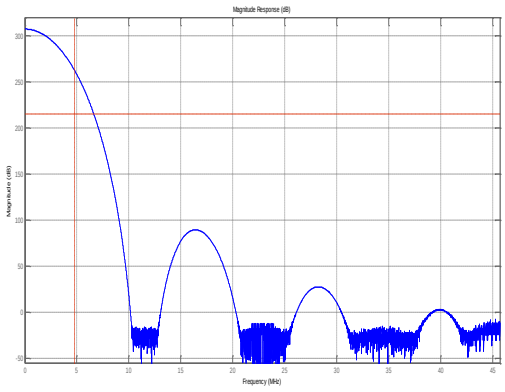

Figure 4: Magnitude response of CIC decimation filter for decimation factor 8

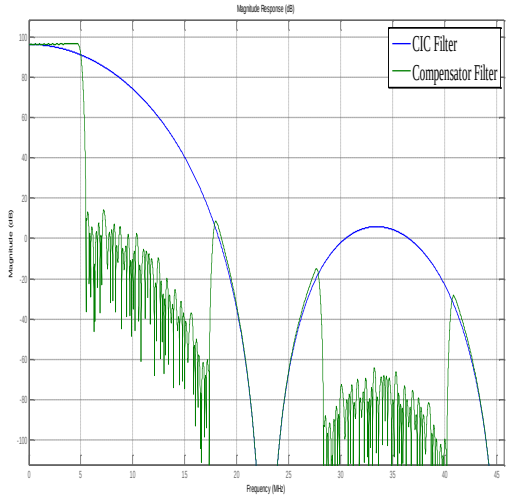

Figure 5: Magnitude response of Cascade design of CIC decimation filter and CIC Compensator for decimation factor 8

TABLE 2: Performance and Implementation Cost Comparison

Parameter	Single Stage CIC Filter	Compensated Two Stage CIC Filter	Compensated Three Stage CIC Filter
Decimation Factor	8	4*2=8	2*2*2=8
Pass band Ripple(dB)	44.02	4.95	1.62
No. of Multipliers	0	120	433
No. of Adders	34	135	456
Multiplication per Input Sample	0	15	54.125
Addition per Input Sample	19.125	24.875	70.5

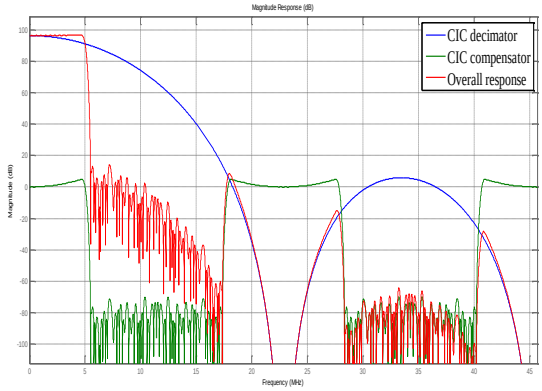

Figure 6: Overall magnitude response of compensated two stage CIC Decimation filter.

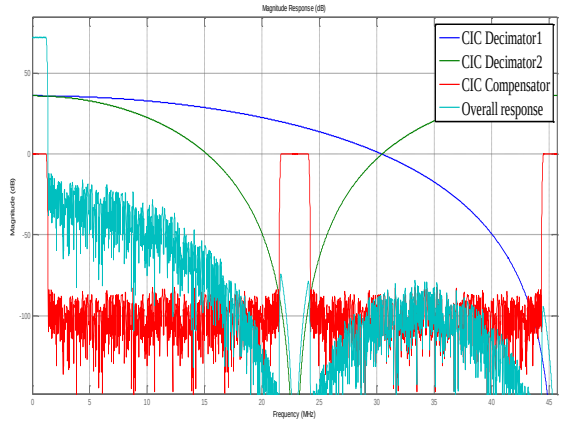

Figure 7: Overall magnitude response of compensated three stages CIC Filter

VI. CONCLUSION

CIC filters are very economic, computationally efficient and simple to implement in comparison with FIR or IIR for large rate change due to lack of multipliers. Decimation of a signal at high frequency using FIR or IIR structures is very complex since it needs a lot of multiplications and hence system cost is increased. This paper analyzed the performance of CIC decimation filter for efficient compensation by using CIC filter as a first stage in decimation when the overall decimation factor is factorized. For overall decimation factor of 8, a sampling rate conversion system is analyzed by cascading different stages of CIC and CIC Compensator filters and found that the cascade design provide the desired passband transition characteristics. It is shown that the cascade designs of CIC filters can help to minimize the amount of passband ripples present in the amplitude response but at the same time implementation cost of the decimation filter is increased which results in more hardware requirement.

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